Amendments to the Claims:

This listing of claims replaces all previous versions and listings of claims in this application:

Listing of Claims:

1-4 (cancelled).

5 (currently amended): A tile-based routing method for routing a plurality of signal traces out of a plurality of corresponding bumper pads in a multi-layer circuit board, the multi-layer circuit board comprising at least a first layer and a second layer, the method comprising:

arranging the plurality of bumper pads as a bumper-tile block by a specific forming process;

assigning [[a]] the plurality of signal traces corresponding to [[a]] the plurality of bumper pads of the bumper-tile block as a plurality of first-layer traces being routed in the first layer;

assigning [[a]] the plurality of signal traces corresponding to [[a]] the plurality of bumper pads of the bumper-tile block as a plurality of second-layer traces being routed in the second layer;

routing the plurality of first-layer traces straight forward;

routing the plurality of second-layer traces with a turn being configured not to be vertically parallel with the plurality of first-layer traces; and

shielding the plurality of first-layer traces and the plurality of second-layer traces.

6 (original): The tile-based routing method of claim 5 further comprising:

arranging a first-layer shielding trace between every two adjacent first-layer traces in the first layer of the multi-layer circuit board; and

arranging a second-layer shielding trace between every two adjacent second-layer traces in the second layer of the multi-layer circuit board.

7 (original): The tile-based routing method of claim 6, wherein the multi-layer circuit board further comprises a third layer used as a ground plane, the method further comprising:

utilizing each first-layer shielding trace connected to the third layer for grounding; and

utilizing each second-layer shielding trace connected to the third layer for grounding.

8 (original): The tile-based routing method of claim 7, wherein the second layer is vertically underneath the first layer, and the third layer is vertically underneath the second layer.

9 (original): The tile-based routing method of claim 5, wherein each bumper-tile block comprises 8 bumper pads, which correspond to 8 signal traces capable of carrying 8 input/output signals, organized in a plurality of triangle units with equal length of each side.

10 (original): The tile-based routing method of claim 9, wherein the bumper-tile block is positioned in a periphery area of a die.

11 (currently amended): The tile-based routing method of claim 5, wherein the plurality of first-layer traces and second-layer traces are routed to a flip chip package by applying ~~being applied to a flip chip packaging technique and other~~ packaging techniques.

12 (original): The tile-based routing method of claim 5, wherein the multi-layer circuit board is a 6-layer build-up substrate or any other multi-layer board for high pin-count application.

13-21 (cancelled).